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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/572,655
Filing Date: March 06, 2007
Appellant(s): EISERT ET AL.

Edward M. Weisz
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 12/23/2010 appealing from the Office action mailed 06/29/2010.

(1) Real Party in Interest

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The following is a list of claims that are rejected and pending in the application:

Claims 1-2, 4-8, 10-18, 44-73.

(4) Status of Amendments After Final

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

(5) Summary of Claimed Subject Matter

The examiner has no comment on the summary of claimed subject matter contained in the brief.

(6) Grounds of Rejection to be Reviewed on Appeal

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being

maintained by the examiner except for the grounds of rejection (if any) listed under the subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

(7) Claims Appendix

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

(8) Evidence Relied Upon

Lester (US 6,291,839)

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 4-8, 10-18, 44-73, are rejected under 35 U.S.C. 103(a) as being unpatentable over Lester (U.S. Patent No. 6,291,839).

Regarding claim 1, Lester discloses in figure 5 a radiation (light) emitting semiconductor chip comprising:

an epitaxial multilayer structure 16, 14, 8, fig. 5 comprising:

an active radiation (light) generating layer 14

a first main face (bottom surface of layer 8) and

a second main face (upper surface of layer 16) remote from the first main face for coupling out radiation generating in the active radiation generating layer 14, and

a reflective layer 9 or interface, and

wherein the first main face of the multilayer structure is coupled to the reflective layer 9 or interface, and

wherein a patterned region 16 of the multilayer structure that adjoins the second main face of the multilayer structure is patterned by either one or two dimensional fig.1 depressions forming convex elevations (truncated pyramids) fig.5.

It is noted that the term "thin film" is a broad limitation herein because there is no recitation of how thin this thin film is in specific. Therefore, the film disclosed by Lester in figure 5 can be construed as "thin film".

Lester discloses the claimed invention except for the convex elevations having a height (h1) at least as large as a distance (h2) between the patterned region and the active, radiation-generating layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the convex elevations of a height (or depth) as taught by Lester (col.5, lines 8-18) to have a height (h1) at least as large as a distance (h2) between the patterned region and the active, radiation-generating layer as of the claimed invention, in order to scatter light in the semiconductor layer and increase the extraction efficiency (col.5, lines 8-18). Furthermore, it has been held that where the

general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In *re Aller*, 105 USPQ 233.

Regarding claim 46, Lester discloses a radiation-emitting thin-film semiconductor chip comprising an epitaxial multilayer structure and a reflective layer or interface, the epitaxial multilayer structure comprising:

an active, radiation-generating layer 14,

a first main face (bottom surface of layer 8), and

a second main face (upper surface of layer 16) remote from the first main face for coupling out the radiation generated in the active, radiation-generating layer 14,

wherein the first main face of the multilayer structure is coupled to the reflective layer 9 or interface, and

wherein a patterned region of the multilayer structure that adjoins the second main face of the multilayer structure is patterned by either one- or two dimensional (figs.1,5) depressions forming convex elevations (truncated pyramids).

It is noted that the term "thin film" is a broad limitation herein because there is no recitation of how thin this thin film is in specific. Therefore, the film disclosed by Lester in figure 5 can be construed as "thin film".

Lester discloses the claimed invention except for the convex elevations having an inclination angle (B) of between approximately 30° and approximately 70°.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the convex elevations having an inclination angle as taught by Lester to the convex elevations having an inclination angle (B) of between approximately 30°and approximately 70° as of the claimed invention, in order to scatter light in the semiconductor layer and increase the extraction efficiency (col.5, lines 8-18). Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In *re Aller*, 105 USPQ 233.

Regarding claims 2, 48, Lester discloses the semiconductor chip as claimed in claim 1, further comprising a carrier element coupled to the first main face, wherein the reflective layer 9 or interface is arranged between the carrier element and the multilayer structure.

It is noted that the substrate as shown in figure 5 can function as "carrier substrate" because it is connected to reflector 9, which enables the substrate to electrically connect with the electrical source or circuit to drive the light emitting device

Regarding claims 4, 5, 49, **50**, Lester discloses in figure 5 the semiconductor chip as claim 1, wherein the elevations of layer 16 have a form of truncated pyramids or truncated cones or a trapezoidal cross sectional form or a form of cones or a triangular cross-section form fig.5.

Regarding claim 6, Lester discloses in figure 5 the elevations 16 have a form of truncated cones, not of a circle or sphere segment cross sectional form as claimed.

However In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966), the Court held that the changes in shape was a matter of choice which a person of ordinary skill in the art would have found obvious absent persuasive evidence (MPEP 2144.04, page 2100-137, Rev. 5, August, 2006).

It would have been obvious to one having ordinary skill in the art at the time of the present invention was made to modify Lester by including the elevation having the circle segment cross sectional form, since this involves only routine skill in the art.

Regarding claims 7, 8, **51**, Lester discloses in figure 5 the elevations have an aperture angle of certain degree(s), not necessarily between approximately 30° and approximately 70° or between approximately 40° and approximately 50°.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Lester by including the elevations having an aperture angle of between approximately 30° and approximately 70° or between approximately 40° and approximately 50°, since it has been held that where the general conditions of a claim are disclosed in the prior art discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claims 10, **52**, **53**, Lester discloses in figure 5 the elevations 16 have certain heights.

Lester does not disclose the height (h1) of the elevations being approximately as large as or twice as large as the distance (h2) between the patterned region of the multilayer structure and the active, radiation generating layer.

It would have been obvious to one having ordinary skill in the art at the time of the invention was made, to modify Lester by including the height of the elevations being approximately twice as large as the distance between the non patterned region of the multilayer structure and the active, radiation generating layer and the elevation, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claims 11, 54, Lester discloses in figure 5 the elevations have a light emitted opening dimension.

Lester does not disclose the cell size (d) of the elevations being at most approximately five times as large as the height (h1)of the elevations.

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify Lester by including a light emitted opening dimension of the elevations being at most approximately five times as large as the height of the elevations, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272,205 USPQ 215 (CCPA 1980).

Regarding claims 12, **55**, Lester discloses in figure 5 the elevations have a light emitted opening dimension.

Lester does not disclose the cell size of the elevations being at most approximately three times as large as the height of the elevations.

It would have been obvious to one having ordinary skill in the art at the time of the invention was made, to modify Lester by including the light emitted opening

dimension of the elevations being at most approximately three times as large as the height of the elevations, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 13, as best understood, Lester discloses in figure 5 the reflective layer 9 or interface coupled to the first main area of the multilayer structure has a reflection at least 70% (column 2, lines 65-66).

Regarding claims 14, **56,** Lester discloses in column 2, lines 65-67 the layer 9 coupled to the first main area of the multilayer structure has a reflection of at least 70%.

Lester does not exclusively discloses a reflectivity of at least 85%.

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify Lester by including the layer or interface couple to the first main area of the multilayer structure as a reflectivity of at least 85%, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 15, Lester discloses in figure 5 the multilayer structure is applied on a carrier substrate (substrate) either directly by its first main face or via a reflective layer.

It is noted that the substrate as shown in figure 5 can function as "carrier substrate" because it is connected to reflector 9, which enables the substrate to electrically connect with the electrical source or circuit to drive the light emitting device.

Regarding claim 16, Lester discloses in figure 5 the reflective layer 9 is also a

conductive layer (col.3 lines 49-50) which can serve as a contact layer of the semiconductor component.

Regarding claim 17, Lester discloses in figure 5 a conductive transparent layer 20 (column 3, lines 41-48) applied onto the second main face of the multilayer structure.2

Regarding claims 18, 60, Lester discloses a conductive transparent chip as claimed in claim 1, further comprising a transparent protective layer 22 (col.4 lines 62-66) applied onto the second main face of the multilayer structure.

Regarding claim 44, Lester discloses the semiconductor chip as claimed in claim 1, wherein each of the convex elevations is defined by two-dimensional depressions fig.1.

Regarding claims 45, 47, Lester discloses the semiconductor chip as claimed in claim 1, wherein the epitaxial multilayer of the semiconductor chip is free of a growth substrate.

Regarding claim 57, Lester discloses the semiconductor chip as claimed in claim 47, wherein the multilayer structure is applied onto a carrier substrate either directly by the first main face or via the reflective layer or interface fig.5.

Regarding claim 58, Lester discloses the semiconductor chip as claimed in claim 57, wherein the reflective layer 9 or interface or the carrier substrate serves as a contact layer of the semiconductor chip, as well known in the art, in order for the

semiconductor chip enables to contact with the electrical source or circuit to drive the light emitting device.

Regarding claim 59, Lester discloses the semiconductor chip as claimed in claim 46, further comprising a conductive, transparent layer 22 (col.4 lines 62-66) applied onto the second main face of the multilayer structure fig.4.

Regarding claim 61, Lester discloses the semiconductor chip as claimed in claim 46, wherein the multilayer structure comprises a material or a plurality of different materials based on GaN (abstract).

Regarding claim 62, Lester discloses the semiconductor chip as claimed in claim 1, wherein the second main face is a noncontinuous layer (the surface has many recess) fig.5.

Regarding claim 63, Lester discloses the semiconductor chip as claimed in claim 1, wherein the reflective layer 9 is in direct contact with the epitaxial multilayer structure fig.5.

Regarding claim 64, Lester discloses the semiconductor chip as claimed in claim 1, wherein the epitaxial multilayer structure is based on a II-VI semiconductor material (GaN, col.5 line27).

Regarding claim 65, Lester discloses the semiconductor chip as claimed in claim 1, wherein the epitaxial multilayer structure is based on a phosphide compound semiconductor material (col.5 line 20).

Regarding claim 66, Lester discloses the semiconductor chip as claimed in claim 1, wherein the epitaxial multilayer structure is based on an arsenide compound semiconductor material (col.5 line 20).

Regarding claim 67, Lester discloses the semiconductor chip as claimed in claim 1, wherein the patterned region of the multilayer structure that adjoins the second main face (top surface of layer 16) of the multilayer structure is patterned by two-dimensional fig.1 depressions forming convex elevations fig.5.

Regarding claim 68, Lester discloses the semiconductor chip as claimed in claim 46, wherein the second main face is a noncontinuous layer (a noncontinuous with recesses) fig.5.

Regarding claim 69, Lester discloses the semiconductor chip as claimed in claim 46, wherein the reflective layer 9 is in direct contact with the epitaxial multilayer structure fig.5.

Regarding claim 70, Lester discloses the semiconductor chip as claimed in claim 46, wherein the epitaxial multilayer structure is based on a II-VI semiconductor material (GaN, col.5 line27).

Regarding claim 71, Lester discloses the semiconductor chip as claimed in claim 46, wherein the epitaxial multilayer structure is based on a phosphide compound semiconductor material (col.5 line 20).

Regarding claim 72, Lester discloses the semiconductor chip as claimed in claim 46, wherein the epitaxial multilayer structure is based on an arsenide compound semiconductor material (col.5 line 20).

Regarding claim 73, Lester discloses the semiconductor chip as claimed in claim 46, wherein the patterned region of the multilayer structure that adjoins the second main face (top surface of layer 16) of the multilayer structure is patterned by two-dimensional fig.1 depressions forming convex elevations fig.5.

(10) Response to Argument

Appellant argues in section Arguments page 4 of the Appeal Brief that *" there are neither one-dimensional nor two-dimensional depressions in Lester, much less ones forming convex elevations" as recited in independent claim 1".*

In response the Examiner respectfully disagrees, because the language of claim 1 is recited as "one or two-dimensional depressions forming convex elevations" which does not distinguish from the one or two-dimensional as taught by Lester's fig.5. Applicant does not specifically determine the characteristic of the one or two-dimensional depressions in the claimed or in light of the specification. For example, in the specification page 11 lines 29-39 to page 12 lines 1-4, Applicant discloses as "*The patterning of the multilayer structure 12 may be formed either one-dimensionally, that is to say with depressions 24 in only one coordinate direction of the plane of the second main face 18, or two-dimensionally, that is to say with depressions 24 in two coordinate directions--preferably running perpendicular to one another--of the plane of the second main face 18*". It would have been obvious for the Examiner and the one of ordinary skill

in the art to interpret the depressions of layer 16 as disclosed in fig.5 by Lester is in one coordinate direction of the plane of the second main face layer 9, or two-dimensionally, with depressions of layer 16 in two coordinate directions--preferably running perpendicular to one another--of the plane of the second main face layer 9 as Applicant's Figure C (page 5 of Appeal Brief). Accordingly, Lester discloses the one-dimension or two-dimension as claimed in claim 1.

Appellant argues in section Arguments page 6 of the Appeal Brief that *"Lester's structure contains concave etched holes formed in the p-type layer 16 (see, also Fig.5 of Lester), rather than convex elevations".*

In response the Examiner respectfully disagrees. As in the American Heritage Dictionary, the meaning of convex is "having a surface or boundary that curves or bulges outward", Lester explicitly discloses in fig.5 a surface that curves or bulges outward of layer 16, therefore, layer 16 can be considered as a convex elevation as same as the convex 26 of the claimed invention. In addition, Applicant does not clearly determine the claimed convex elevations is in a top view or in a cross section view.

Appellant argues in section Arguments page 7 of the Appeal Brief that "*claim 62 recites " the second main face is a noncontinuous layer". In contrast, the second main face of Lester's device is a continuous layer (see Figure C of the enclosed illustration)".*

In response the Examiner respectfully disagrees, because the Applicant does not determine the characteristic of the noncontinuous face. As in the rejection above, the Examiner calls the upper surface of layer 16 in Lester's fig. 5 is the main face. It is very

obvious to see that the surface of layer 16 has many recess area which make the face of layer 16 is noncontinuous surface.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/C. N. L./

Examiner, Art Unit 2811

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